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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,666	09/18/2003	Douglas R. Hackler SR.	51889/5	4619

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John R. Thompson
STOEL RIVES LLP
One Utah Center
201 South Main Street, Suite 1100
Salt Lake City, UT 84111

EXAMINER	
THOMAS, ERIC W	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,666	HACKLER ET AL.	
	Examiner	Art Unit	
	Eric W Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/21/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *13-25 and 39-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 26-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of invention I in the reply filed on 6/21/04 is acknowledged. The traversal is on the ground(s) that the capacitor as claimed cannot be formed without an etching process. This is not found persuasive because applicant does not disclose the capacitor must be "microlevel" in size. The capacitor as claimed can be formed by macro level fabrication (does not require the step of etching), the trench can be formed by a drill, and the capacitor as claimed does not require the step of depositing a sacrificial material in the trench.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

2. Claim 31is objected to because of the following informalities:

Claim 31, line 1, the limitation, "The capacitor structure of claim 22" is confusing. Claim 22 is drawn to a method of forming the capacitor. The examiner interpreted this claim as if it depended on claim 26. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-9, 11-12, 26-29, 31-34, 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawakubo et al. (US 5,952,687).

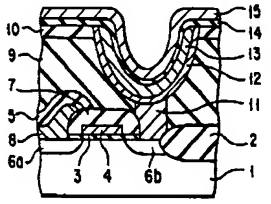


FIG. 3

Kawakubo et al. disclose in fig. 3, a capacitor structure, comprising a substrate (1), an insulating material (9) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench; a bottom electrode (13), wherein the bottom electrode is formed onto the capacitor trench so as to form a layer within the capacitor trench, wherein the bottom electrode extends up the sides of the capacitor trench to form bottom electrode sidewalls, a capacitor dielectric (13) positioned on the bottom electrode, and a top electrode (15) positioned on the capacitor dielectric.

Regarding claim 2, Kawakubo et al. disclose the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material (col. 4 lines 53-60 & col. 7 lines 25-35).

Regarding claim 3, Kawakubo et al. disclose the capacitor has a high-k dielectric constant (col. 4 lines 53-55).

Regarding claim 4, Kawakubo et al. disclose the capacitor dielectric has a dielectric constant greater than 6.0 (the dielectric used has a dielectric constant higher than 100).

Regarding claim 6, Kawakubo et al. disclose the capacitor structure is a discrete capacitor.

Regarding claim 7, Kawakubo et al. disclose the capacitor structure is configured to be part of an integrated circuit.

Regarding claim 8, Kawakubo et al. disclose a conductive material (12) layer, wherein the conductive material layer is in contact with the bottom electrode.

Regarding claim 9, Kawakubo et al. disclose the conductive material layer is a different material than the bottom electrode (col. 7 lines 48-59).

Regarding claim 10, Kawakubo et al. disclose the top electrode is disposed in the capacitor trench such that the top electrode interdigitates with the bottom electrode.

Regarding claim 11, Kawakubo et al. disclose the bottom electrode further comprises a bottom electrode top wall.

Regarding claim 12, Kawakubo et al. disclose the bottom electrode further comprises a bottom electrode base.

Regarding claim 26, Kawakubo et al. disclose a capacitor structure, comprising a substrate (1); an insulating material (9) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench, a bottom electrode (13), wherein the bottom electrode comprises a bottom electrode layer in the capacitor trench and a bottom electrode plug (11) disposed within the capacitor trench, wherein the bottom electrode layer extends up the sides of the capacitor trench to form bottom electrode sidewalls, a capacitor dielectric (14) positioned on the bottom electrode, and a top electrode (15) positioned on the capacitor dielectric.

Regarding claim 27, Kawakubo et al. disclose the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material.

Regarding claim 28, Kawakubo et al. disclose the capacitor dielectric has a high-k dielectric constant.

Regarding claim 29, Kawakubo et al. disclose the capacitor dielectric has a dielectric constant is greater than 100.

Regarding claim 31, Kawakubo et al. disclose the capacitor structure is a discrete capacitor.

Regarding claim 32, Kawakubo et al. disclose the capacitor structure is configured to be part of an integrated circuit.

Regarding claim 33, Kawakubo et al. disclose a conductive material (12) layer, wherein the conductive material layer is in contact with the bottom electrode.

Regarding claim 34, Kawakubo et al. disclose the conductive material layer is a different material than the bottom electrode (col. 7 lines 48-59).

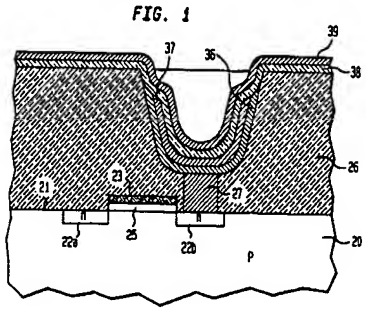
Regarding claim 35, Kawakubo et al. disclose the bottom electrode and the capacitor dielectric are formed in a shape of a box (see fig. 5E)

Regarding claim 36, Kawakubo et al. disclose the top electrode is disposed in the capacitor trench such that the top electrode interdigitates with the bottom electrode.

Regarding claim 37, Kawakubo et al. disclose the bottom electrode further comprises a bottom electrode top wall.

Regarding claim 38, Kawakubo et al. disclose the bottom electrode further comprises a bottom electrode base.

5. Claims 1 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Gutsche (US 6,437,387).



Gutsche discloses in fig. 1, a capacitor structure, comprising a substrate (20), an insulating material (26) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench; a bottom electrode (37), wherein the bottom electrode is formed onto the capacitor trench so as to form a layer within the capacitor trench, wherein the bottom electrode extends up the sides of the capacitor trench to form bottom electrode sidewalls, a capacitor dielectric (38) positioned on the bottom electrode, and a top electrode (39) positioned on the capacitor dielectric.

Regarding claim 26, Gutsche discloses a capacitor structure, comprising a substrate (20); an insulating material (26) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench, a bottom electrode (37), wherein the bottom electrode comprises a bottom electrode layer in the capacitor trench and a bottom electrode plug (27) disposed within the capacitor trench, wherein the bottom electrode layer extends up the sides of the capacitor trench to form bottom

electrode sidewalls, a capacitor dielectric (38) positioned on the bottom electrode, and a top electrode (39) positioned on the capacitor dielectric.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 5, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutsche (US 6,437,387) in view of Alers et al. (US 6,320,244).

Regarding claims 5 and 30, Gutsche discloses the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. Teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Gutsche, since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5,656,852 – discloses a capacitor having multiple dielectric layers.

5,576,928 – discloses a capacitor having increased surface area wherein the dielectric is formed from multiple layers.

In order to ensure full consideration of any amendments, affidavits, or declaration, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1. 116 which will be strictly enforced.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric W Thomas
Examiner
Art Unit 2831

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